

IN THE SPECIFICATION

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2 Replace the paragraph starting on Page ¹¹8, line ¹¹~~18~~, with the following paragraph:

3 Referring now to Figure 3, and as mentioned earlier, the ISOC 120 comprises a first memory
4 space 220 and 230 and a second memory space 240 and the adapter 80 further comprises a third
5 level memory 250. The first, second, and third memory spaces for part of a memory subsystem
6 210 of the adapter 80. In a preferred embodiment of the present invention, the ISOC 120
7 comprises a TX processor (TX MPC) 150 dedicated to data transmission operations and an RX
8 processor (RX MPC) 160 dedicated to data reception operation. In particularly preferred
9 embodiments of the present invention, processors 150 and 160 are implemented by Reduced
10 Instruction Set Computing (RISC) microprocessors such as IBM PowerPC 405 RISC
11 microprocessors. Within the memory subsystem 210, the ISOC 120 comprises, in addition to the
12 first and second memory spaces, a data cache 180 and an instruction cache ~~170~~ 175 associated
13 with TX processor 150, together with a second data cache 190 and second instruction cache 190
14 associated with RX processor 160. The difference between the three levels is the size of memory
15 and the associated access time. As will become apparent shortly, the memory subsystem 210
16 facilitates convenient access to instruction and data by both the TX processor 150 and the RX
17 processor 160; scaleability; and sharing of resources between the TX processor 150 and the RX
18 processor 160 in the interests of reducing manufacturing costs.